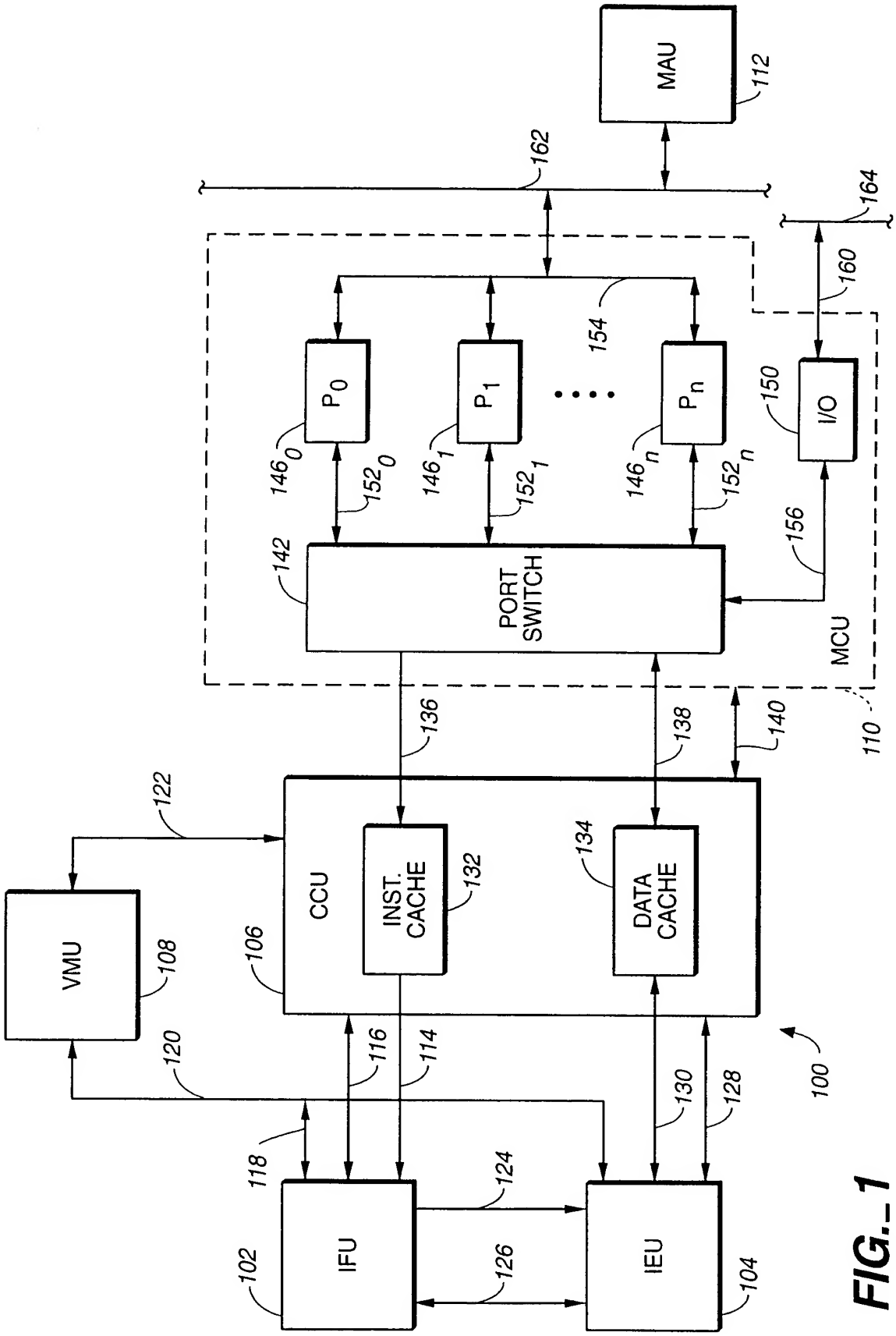
MAU
112
162
164
160
154
P_0
P_1
P_n
I/O
150
146_0
146_1
146_n
152_0
152_1
152_n
142
PORT SWITCH
156
MCU
110
136
138
140
122
CCU
INST. CACHE
132
DATA CACHE
134
VMU
108
106
120
116
114
130
128
100
118
124
126
IFU
IEU
102
104

FIG._1

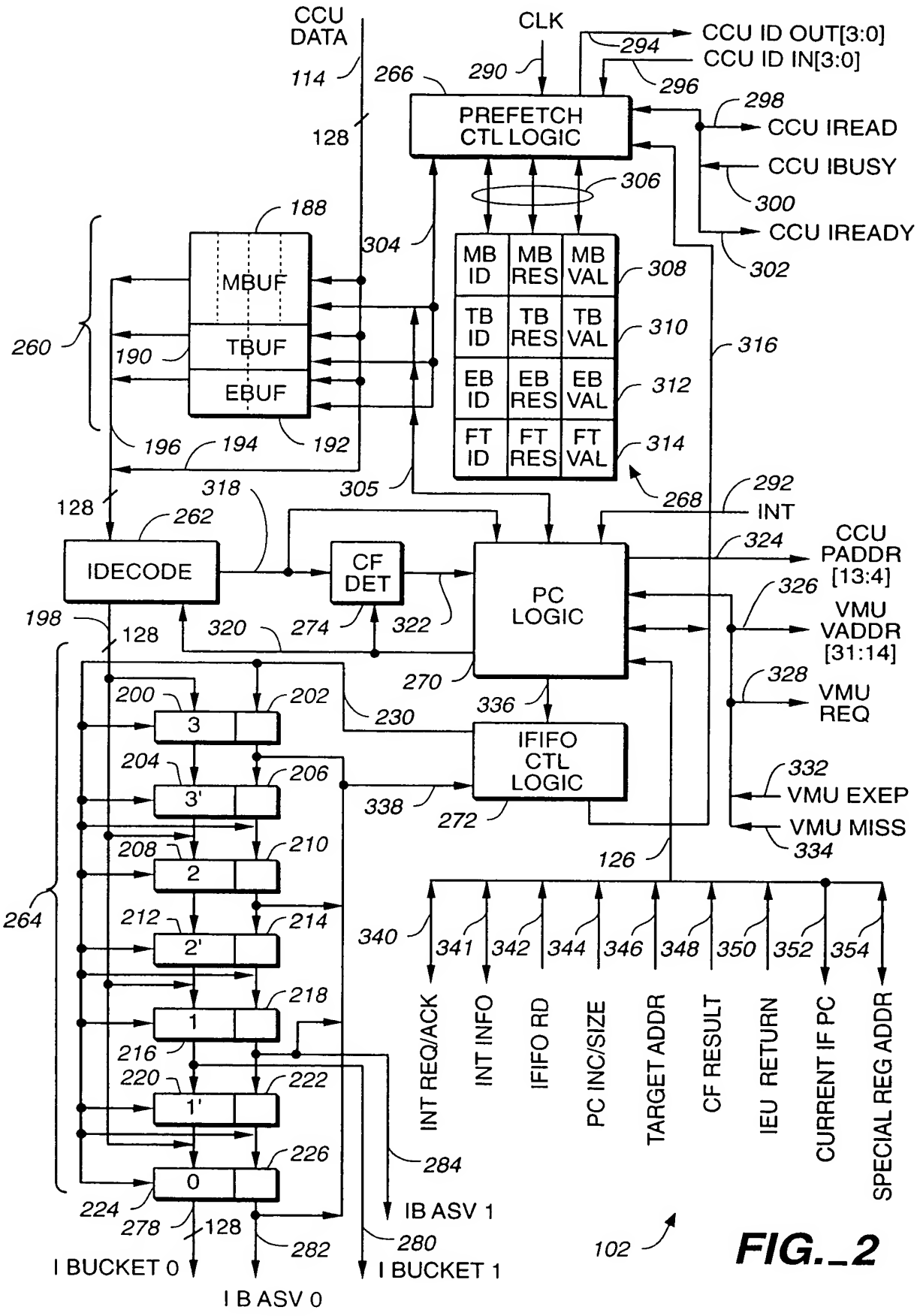
CCU DATA
114
128
CLK
290
266
PREFETCH CTL LOGIC
294
CCU ID OUT[3:0]
296
CCU ID IN[3:0]
298
CCU IREAD
CCU IBUSY
300
CCU IREADY
302
306
188
304
MBUF
TBUF
EBUF
260
190
196
194
192
MB ID
MB RES
MB VAL
308
TB ID
TB RES
TB VAL
310
EB ID
EB RES
EB VAL
312
FT ID
FT RES
FT VAL
314
316
305
268
292
INT
318
128
262
IDECODE
CF DET
PC LOGIC
324
CCU PADDR [13:4]
326
VMU VADDR [31:14]
328
VMU REQ
198
320
274
322
270
336
IFIFO CTL LOGIC
338
272
332
VMU EXEP
VMU MISS
334
126
200
202
230
3
204
206
3'
208
210
2
212
214
2'
218
1
216
220
222
1'
226
0
224
278
282
284
280
IB ASV 1
I BUCKET 1
I BUCKET 0
I B ASV 0
264
340
341
342
344
346
348
350
352
354
INT REQ/ACK
INT INFO
IFIFO RD
PC INC/SIZE
TARGET ADDR
CF RESULT
IEU RETURN
CURRENT IF PC
SPECIAL REG ADDR
102

FIG._2

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Title: High-Performance, Superscalar-Based Computer System With Out-Of-Order Instruction Execution
Replacement Sheet

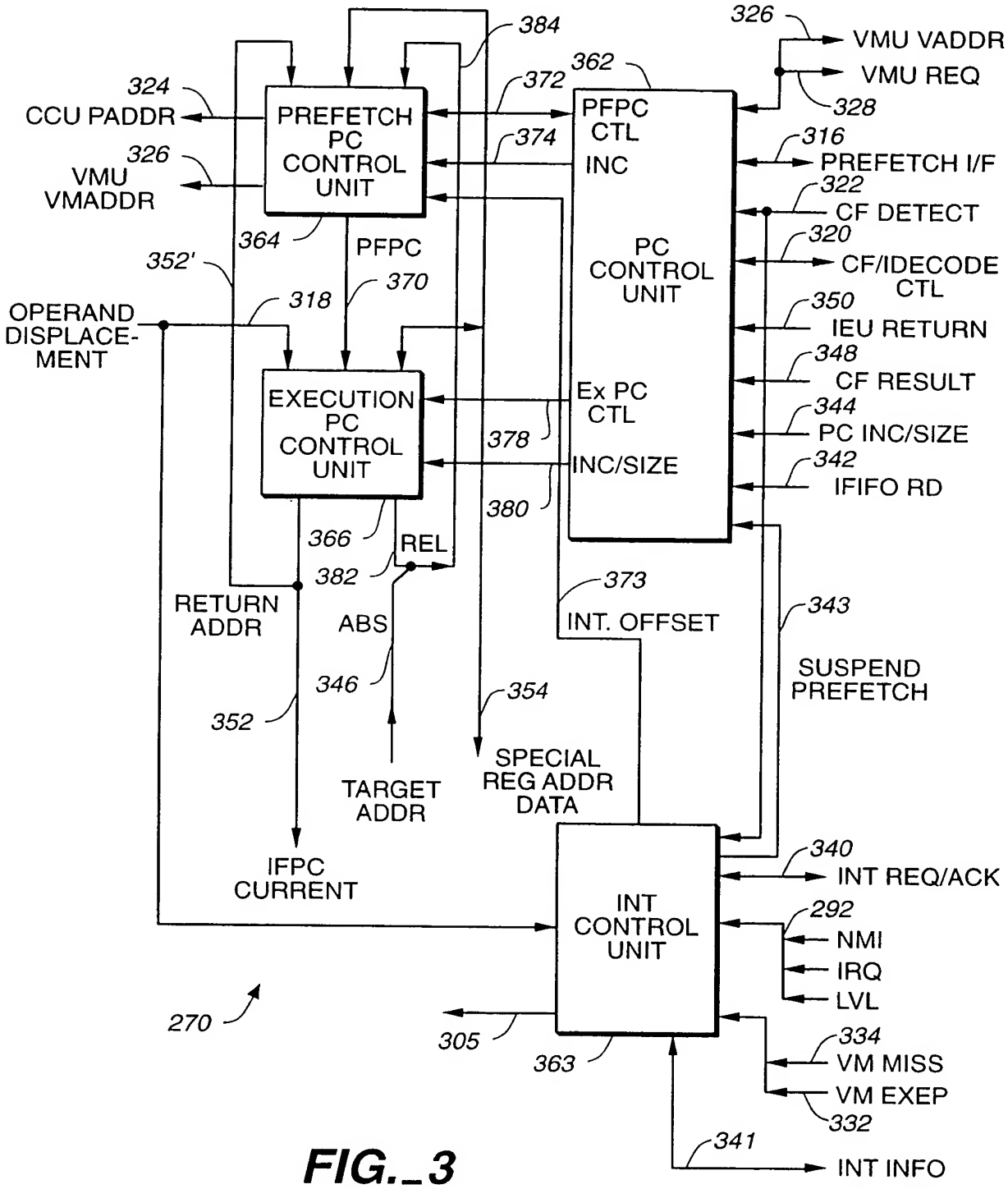

FIG._3

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Inventor(s): NGUYEN et al.; Tel: 202/371-2600
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Replacement Sheet

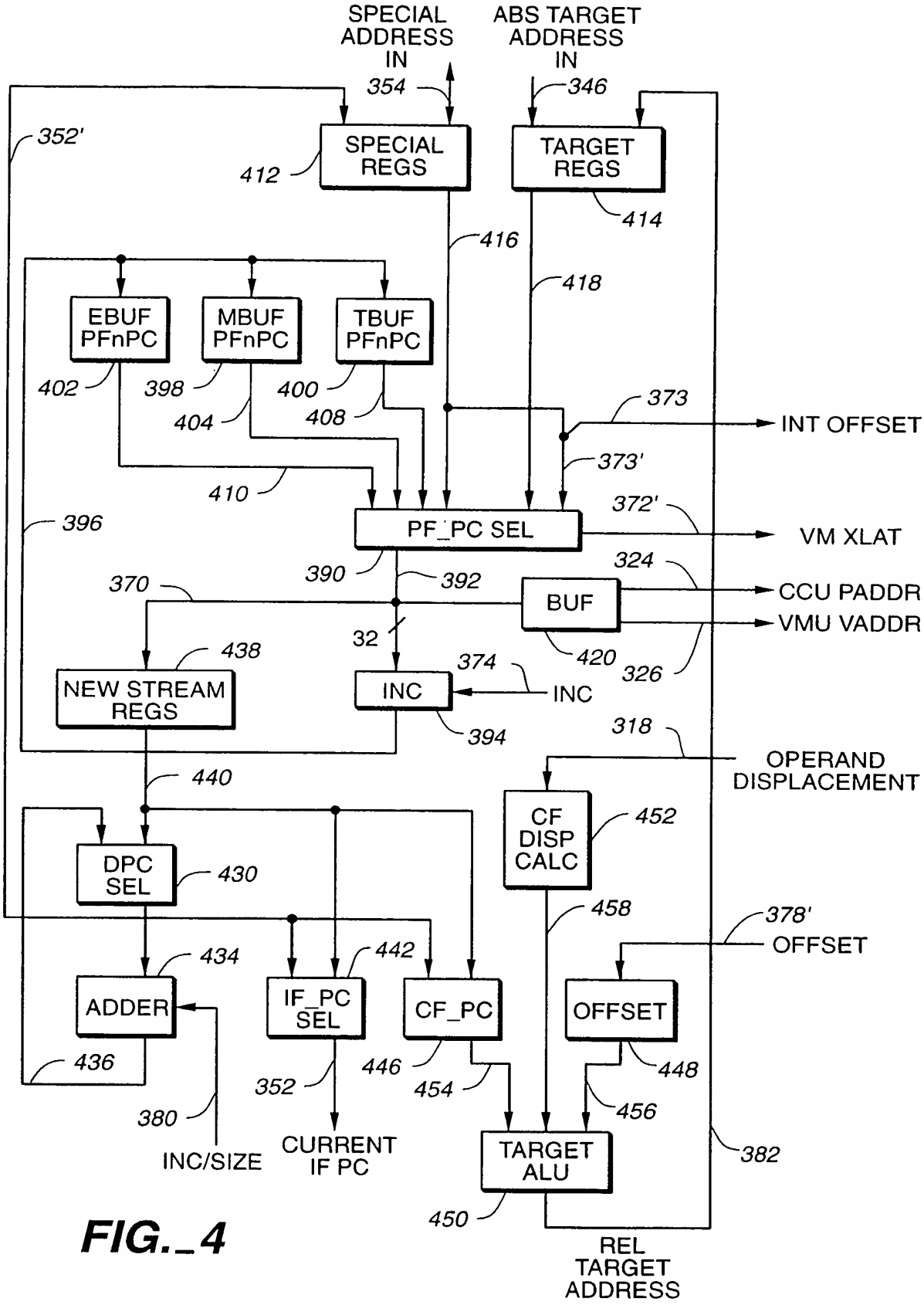

FIG._4

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Title: High-Performance, Superscalar-Based Computer System With Out-Of-Order Instruction Execution
Replacement Sheet

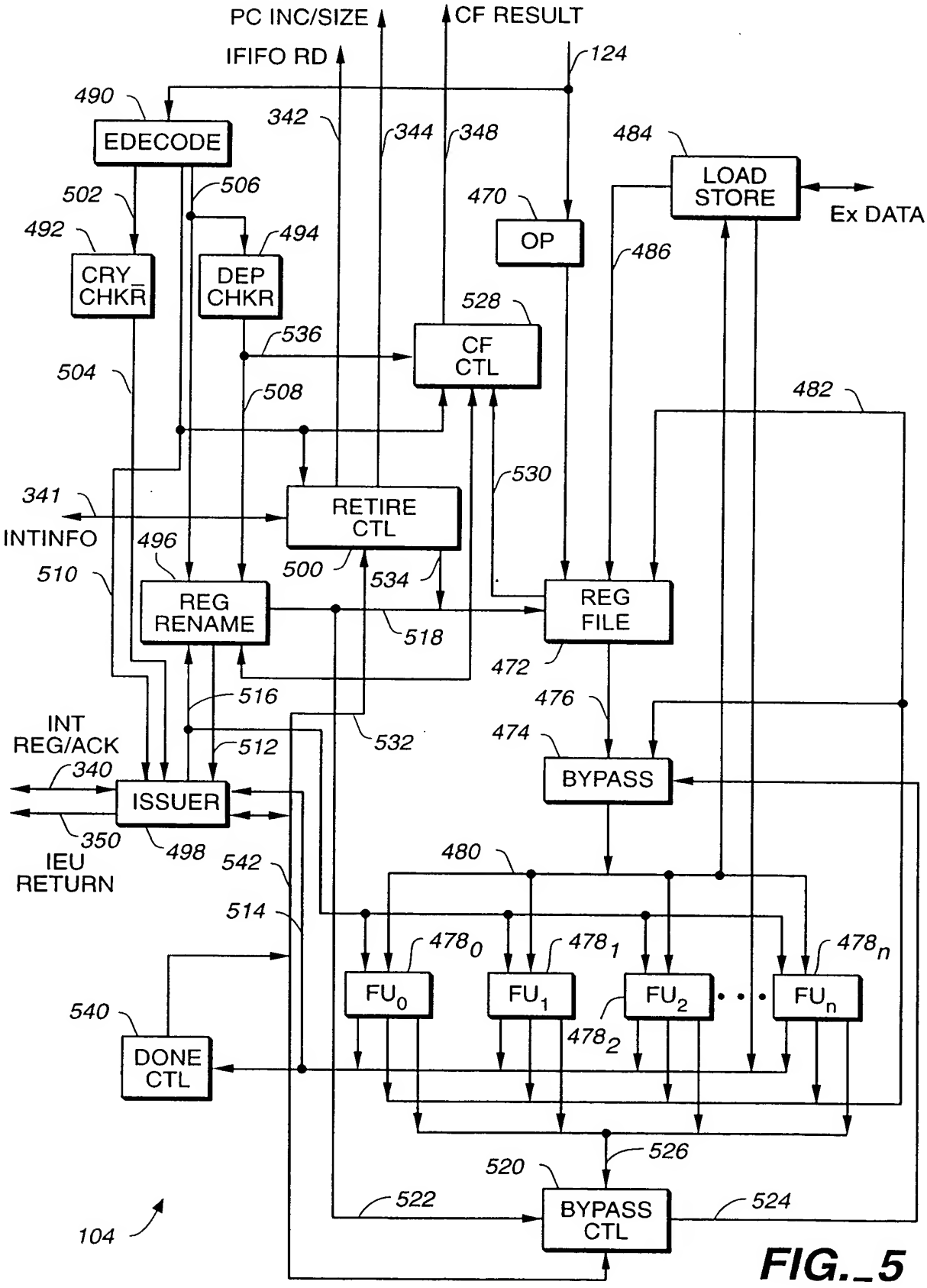

FIG._5

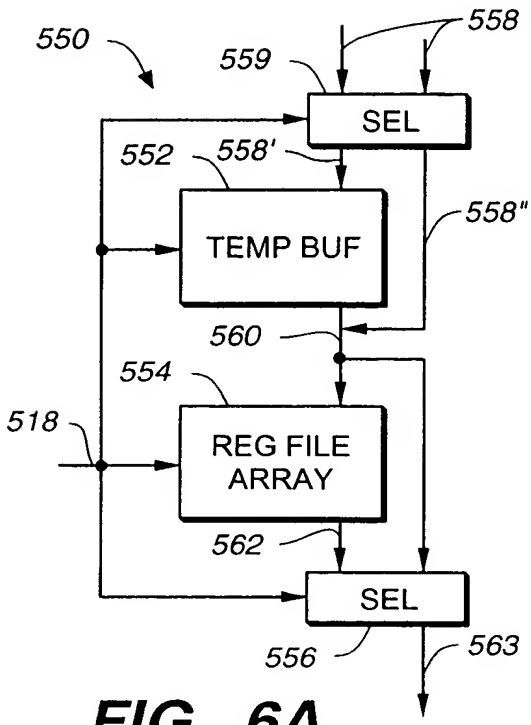

FIG._6A

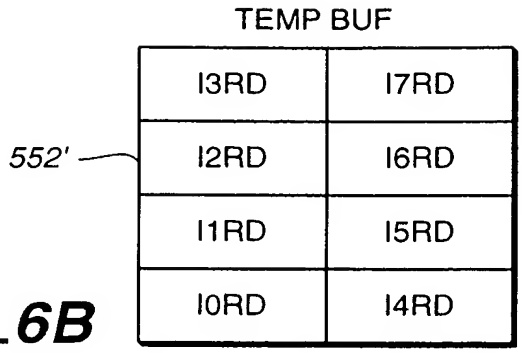

FIG._6B

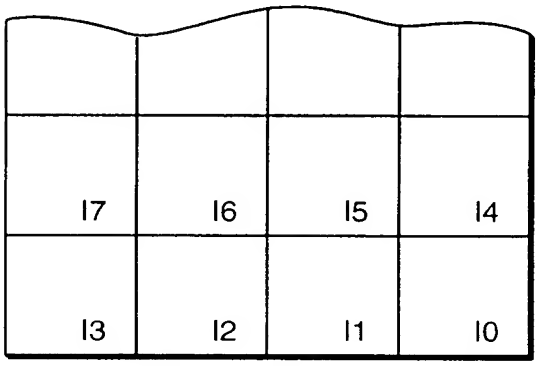

FIG._6C

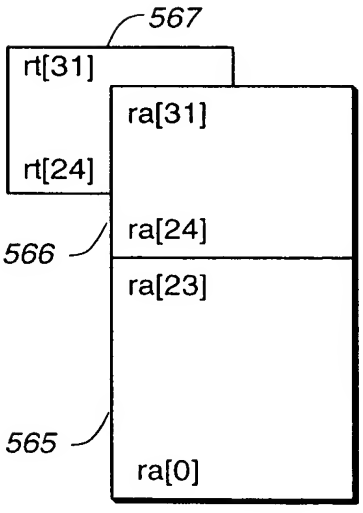

FIG._7A

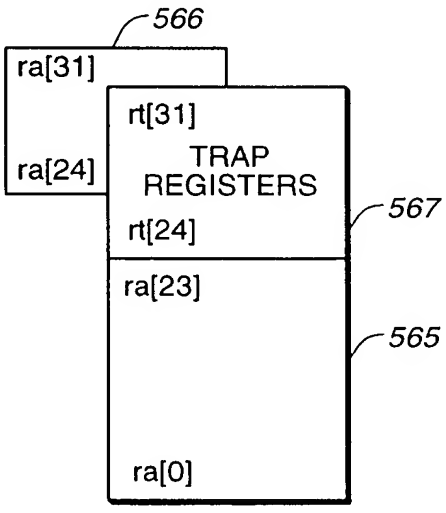

FIG._7B

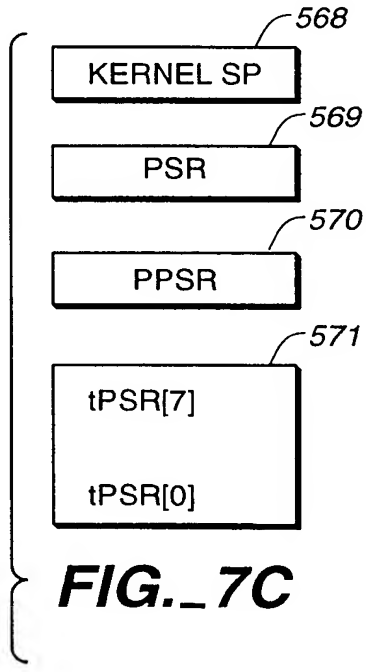

FIG._7C

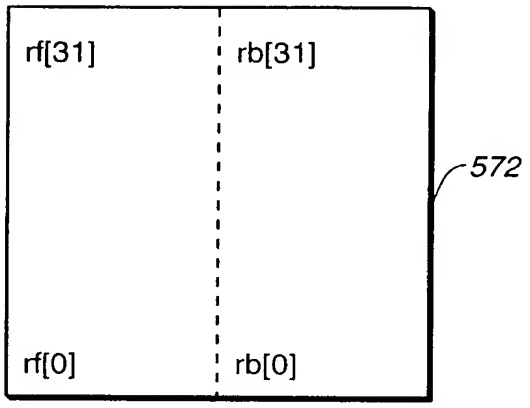

FIG._8

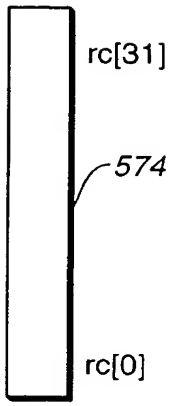

FIG._9

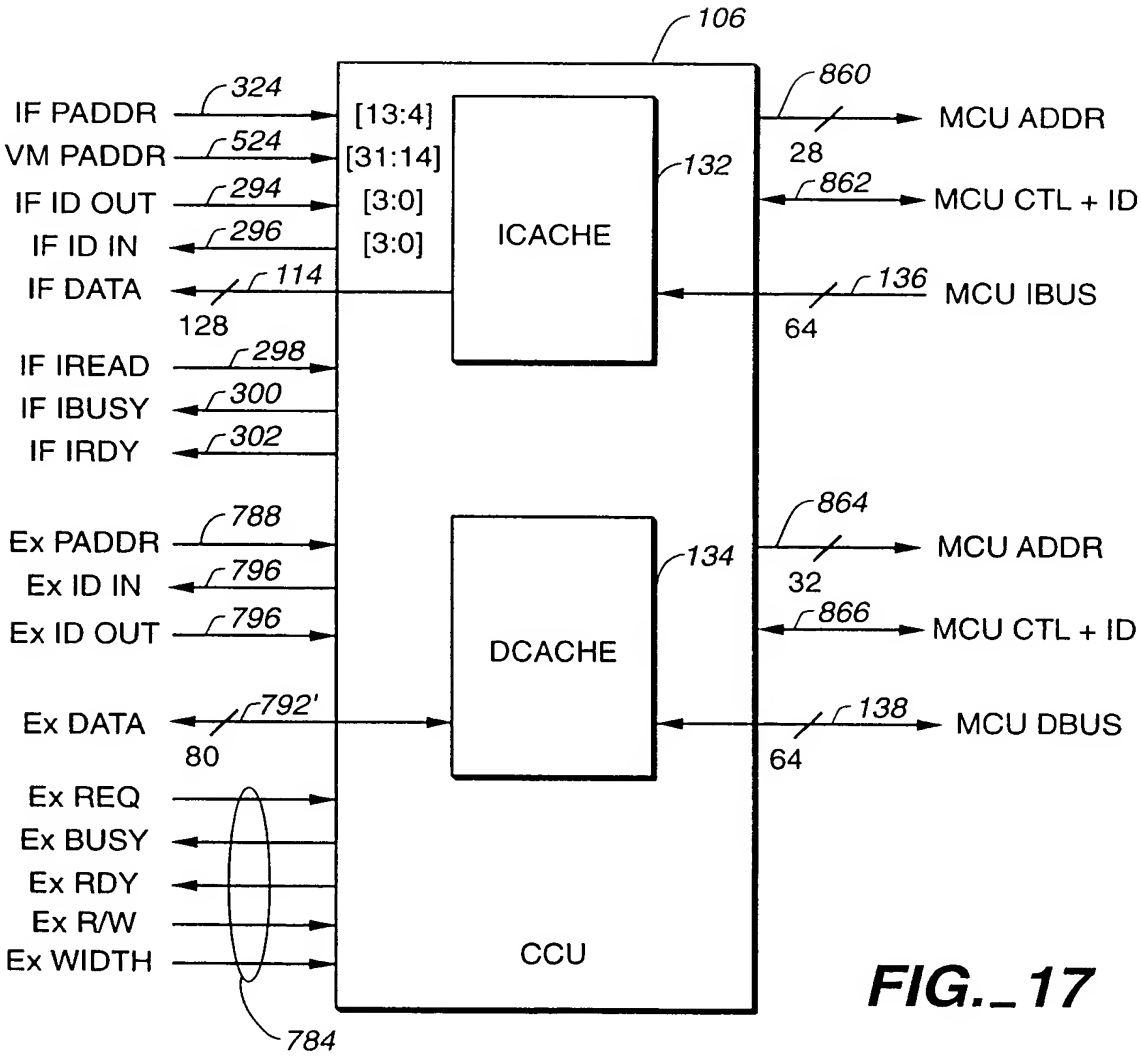

FIG._17

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Inventor(s): NGUYEN et al.; Tel: 202/371-2600
Title: High-Performance, Superscalar-Based Computer System With Out-Of-Order Instruction Execution
Replacement Sheet

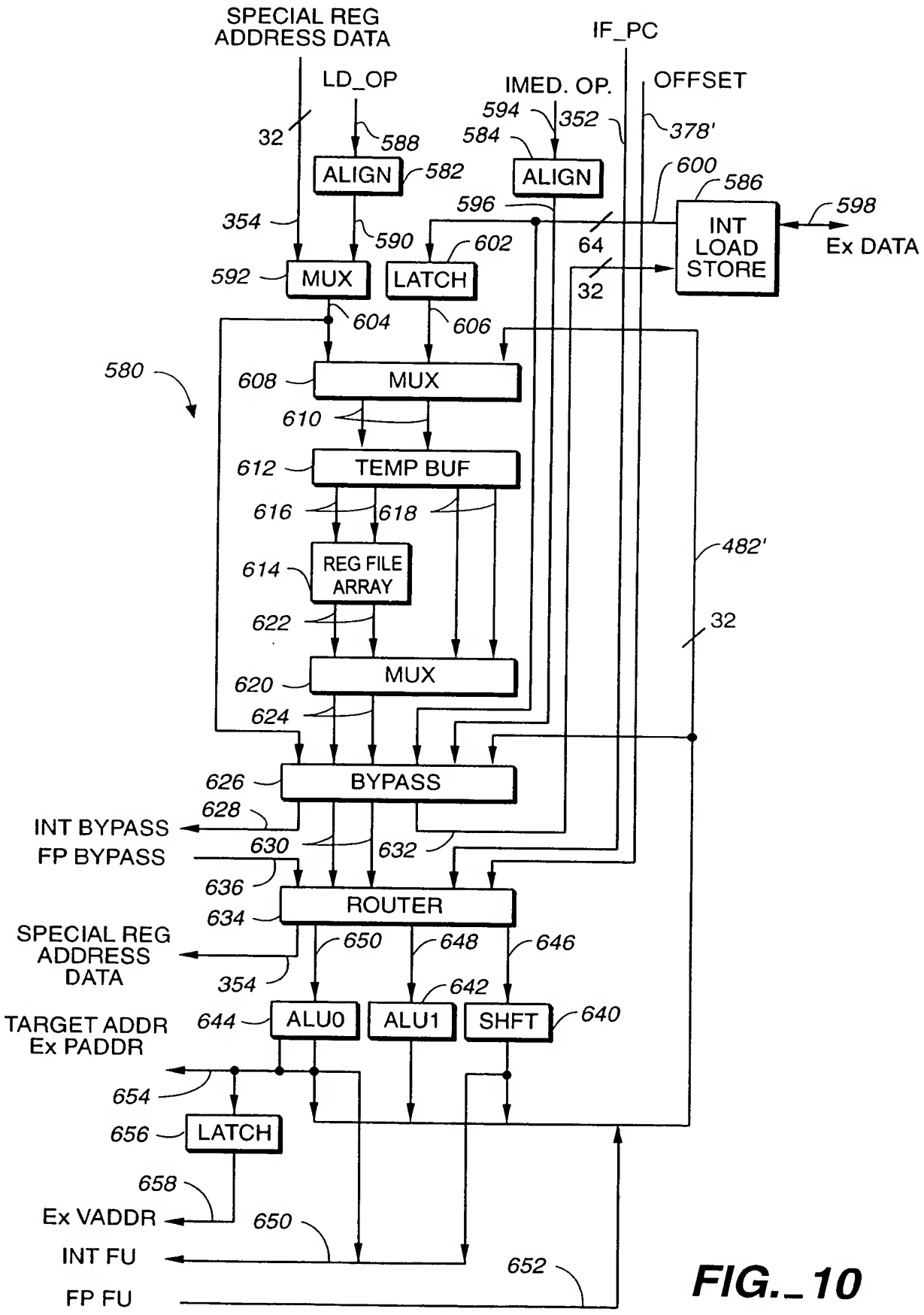

FIG._10

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Dkt. No. SP015.C18; Group Art Unit: TBA
Inventor(s): NGUYEN et al.; Tel: 202/371-2600
Title: High-Performance, Superscalar-Based Computer System With Out-Of-Order Instruction Execution
Replacement Sheet

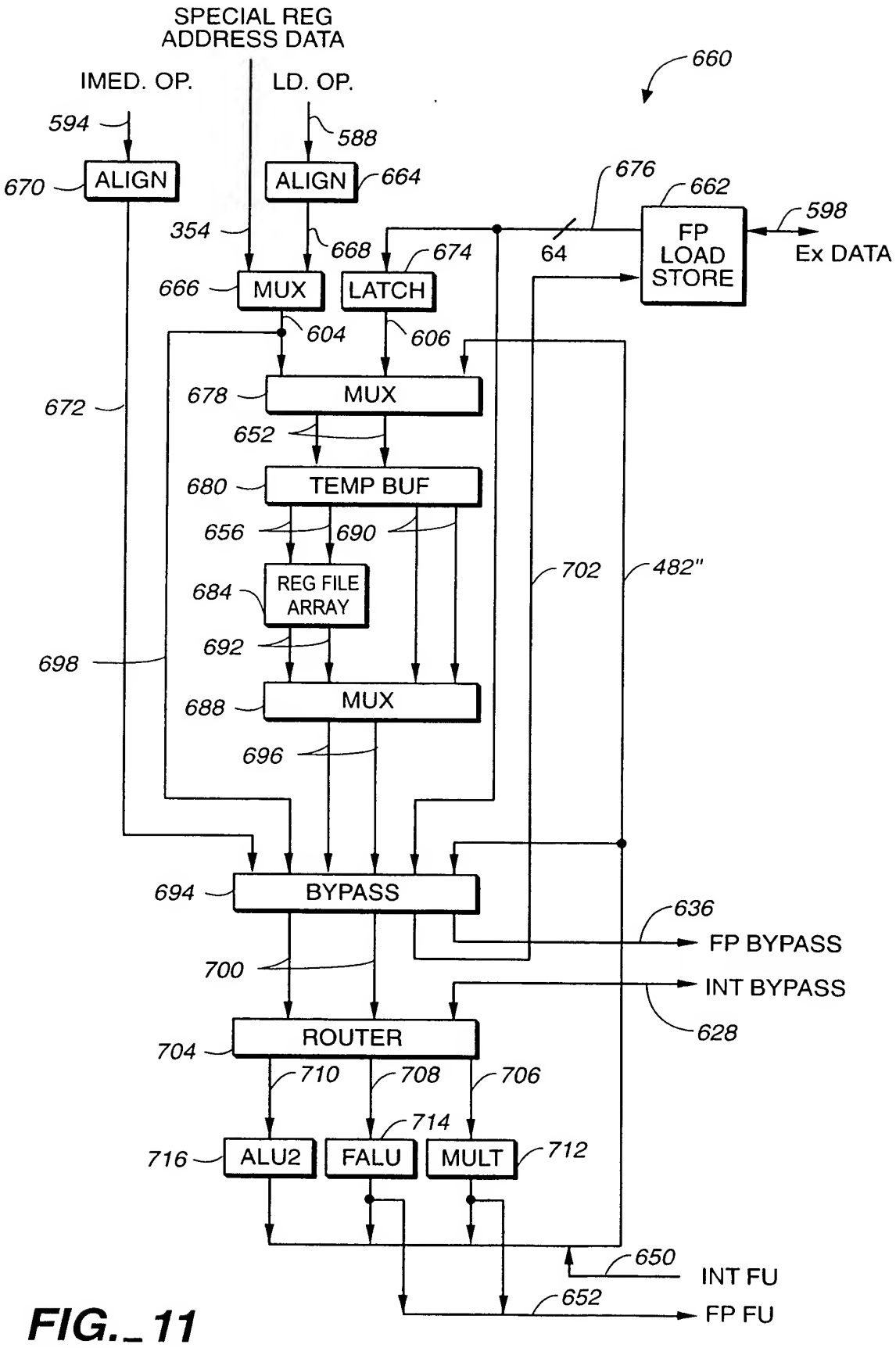

FIG._11

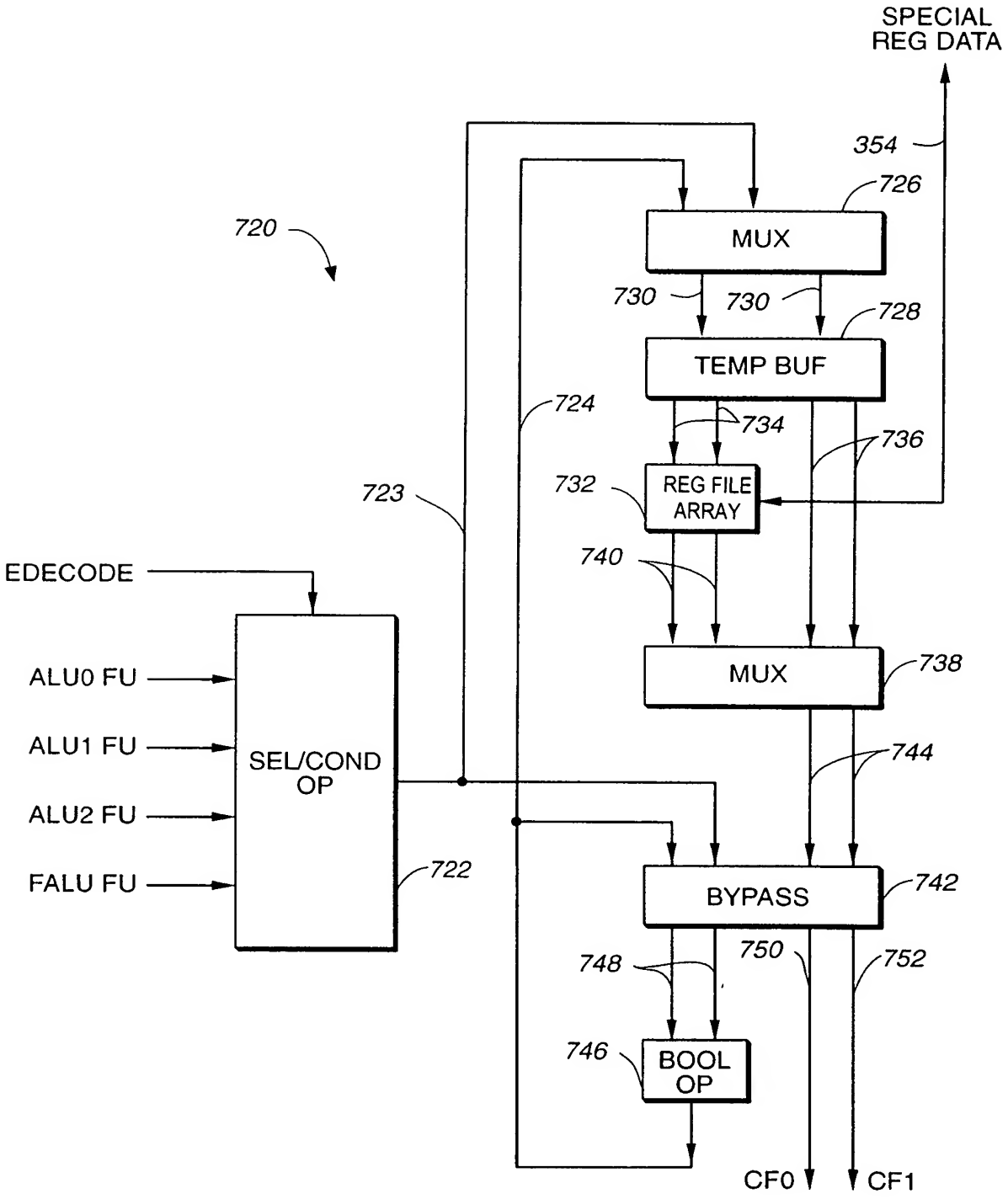
SPECIAL REG DATA
354
726
MUX
720
730
730
728
TEMP BUF
724
734
736
723
732
REG FILE ARRAY
740
EDECODE
MUX
738
ALU0 FU
ALU1 FU
ALU2 FU
FALU FU
SEL/COND OP
744
722
BYPASS
742
748
750
752
746
BOOL OP
CF0
CF1

FIG._12

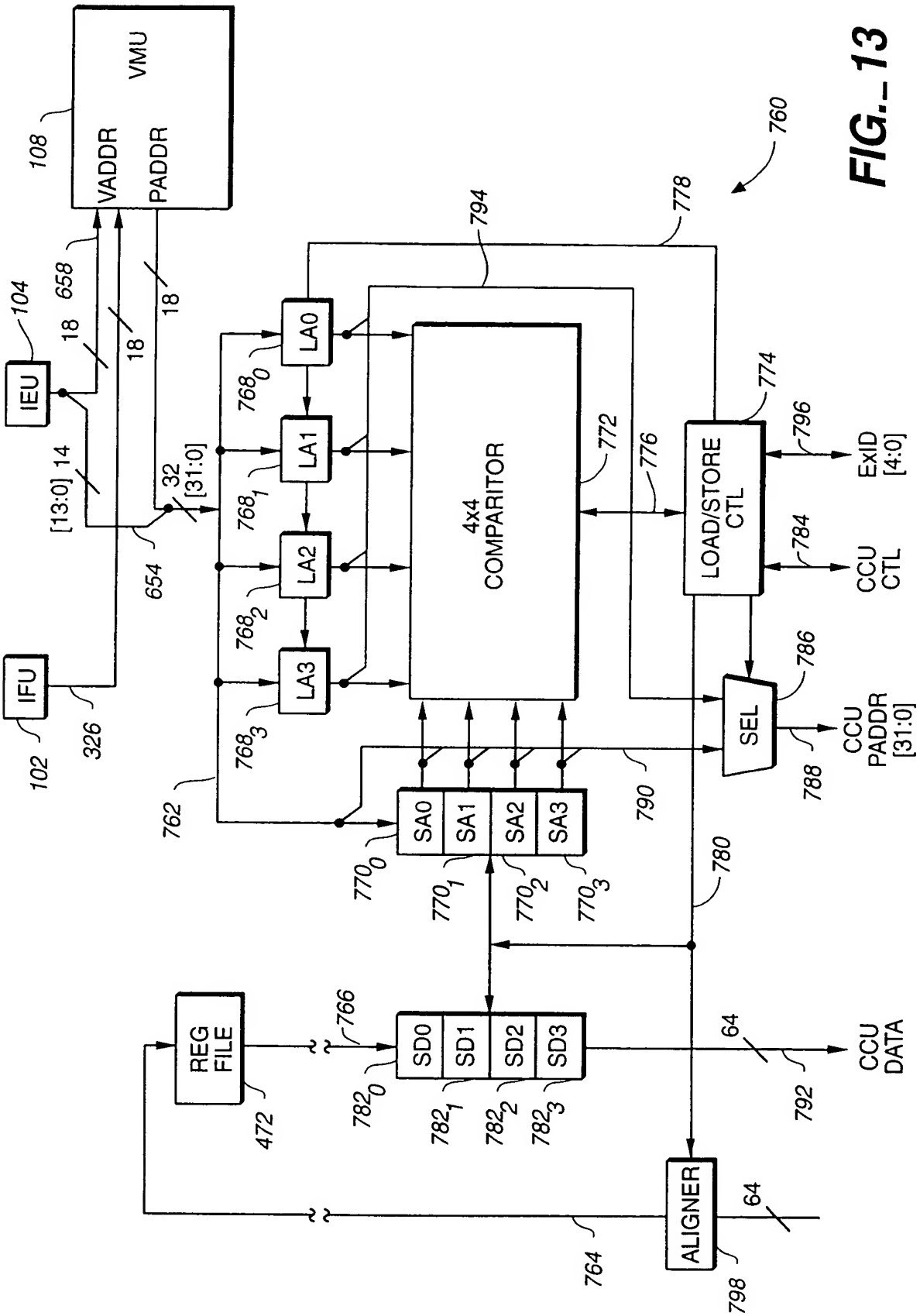
VMU
VADDR
PADDR
108
658
18
18
18
104
IEU
[13:0] 14
654
32 [31:0]
102
IFU
326
LA0
LA1
LA2
LA3
768$_0$
768$_1$
768$_2$
768$_3$
762
4x4 COMPARITOR
772
776
794
778
760
LOAD/STORE CTL
774
796
ExID [4:0]
784
CCU CTL
SEL
786
CCU PADDR [31:0]
788
790
SA0
SA1
SA2
SA3
770$_0$
770$_1$
770$_2$
770$_3$
780
REG FILE
472
766
SD0
SD1
SD2
SD3
782$_0$
782$_1$
782$_2$
782$_3$
64
CCU DATA
792
ALIGNER
64
764
798

FIG._13

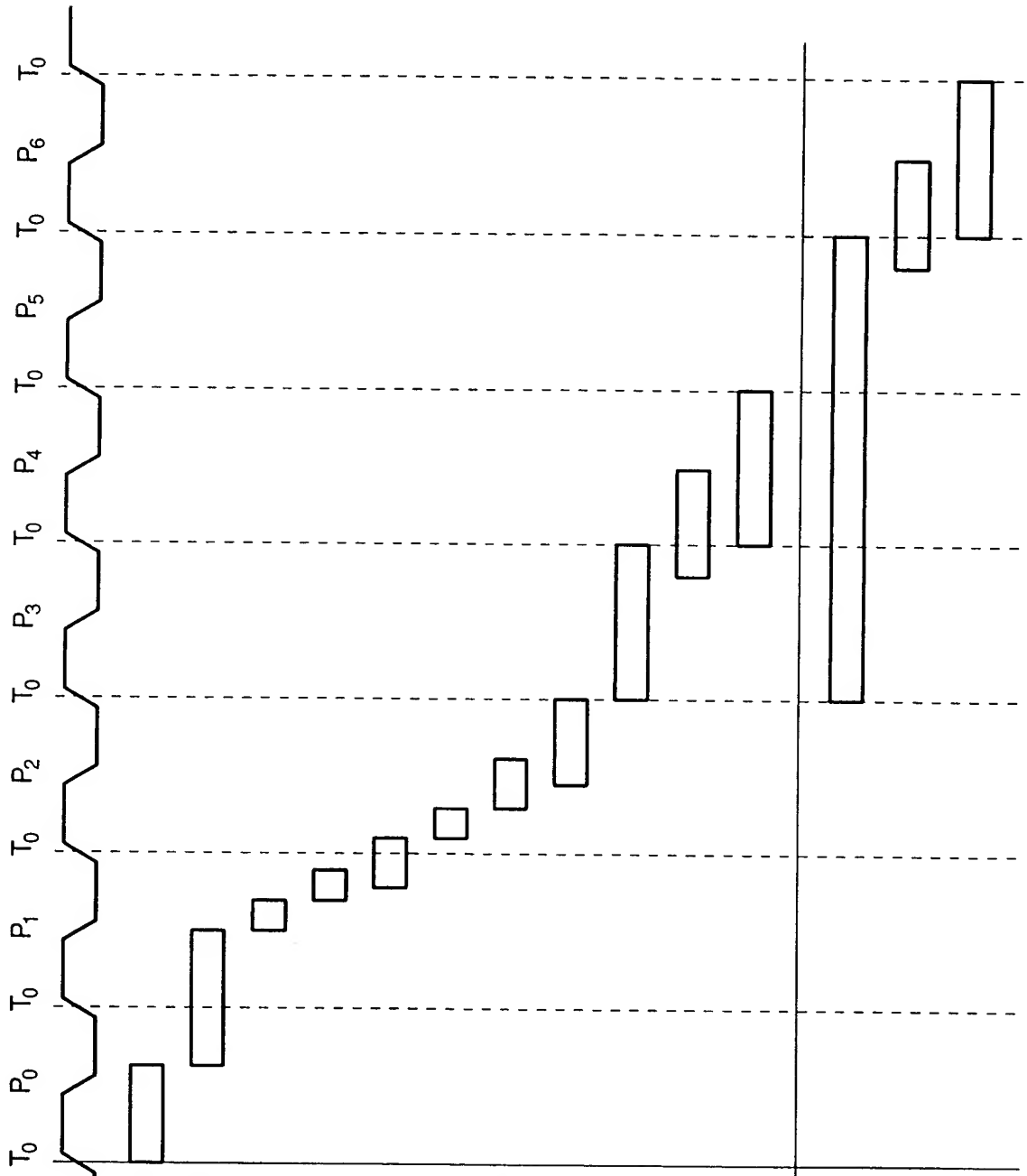
T0
P0
T0
P1
T0
P2
T0
P3
T0
P4
T0
P5
T0
P6
T0
ADDR CALC
ICACHE ACCESS
IBUFFER
EDECODE
DATA DEP
REG RENAME
INS ISSUER
RFILE ACCESS
EXECUTE 0
OUTPUT 0
STORE 0
EXECUTE 1
OUTPUT 1
STORE 1

FIG._14

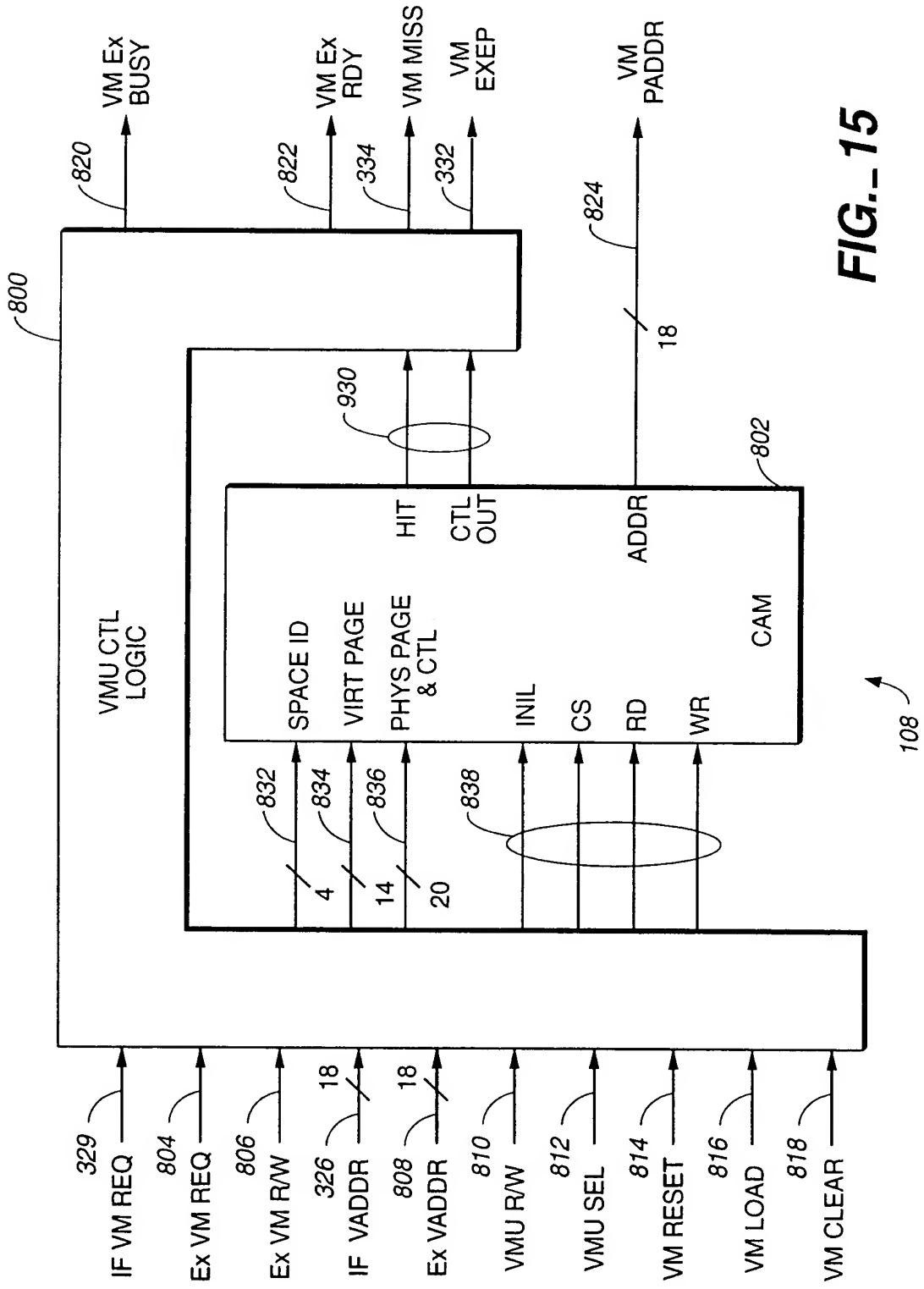
800
VMU CTL LOGIC
820
VM Ex BUSY
822
VM Ex RDY
334
VM MISS
332
VM EXEP
824
VM PADDR
18
930
802
HIT
CTL OUT
ADDR
SPACE ID
VIRT PAGE
PHYS PAGE & CTL
INIL
CS
RD
WR
CAM
832
834
836
838
4
14
20
108
329
IF VM REQ
804
Ex VM REQ
806
Ex VM R/W
326
IF VADDR
18
808
Ex VADDR
18
810
VMU R/W
812
VMU SEL
814
VM RESET
816
VM LOAD
818
VM CLEAR

FIG._15

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Inventor(s): NGUYEN et al.; Tel: 202/371-2600
Title: High-Performance, Superscalar-Based Computer System With Out-Of-Order Instruction Execution
Replacement Sheet

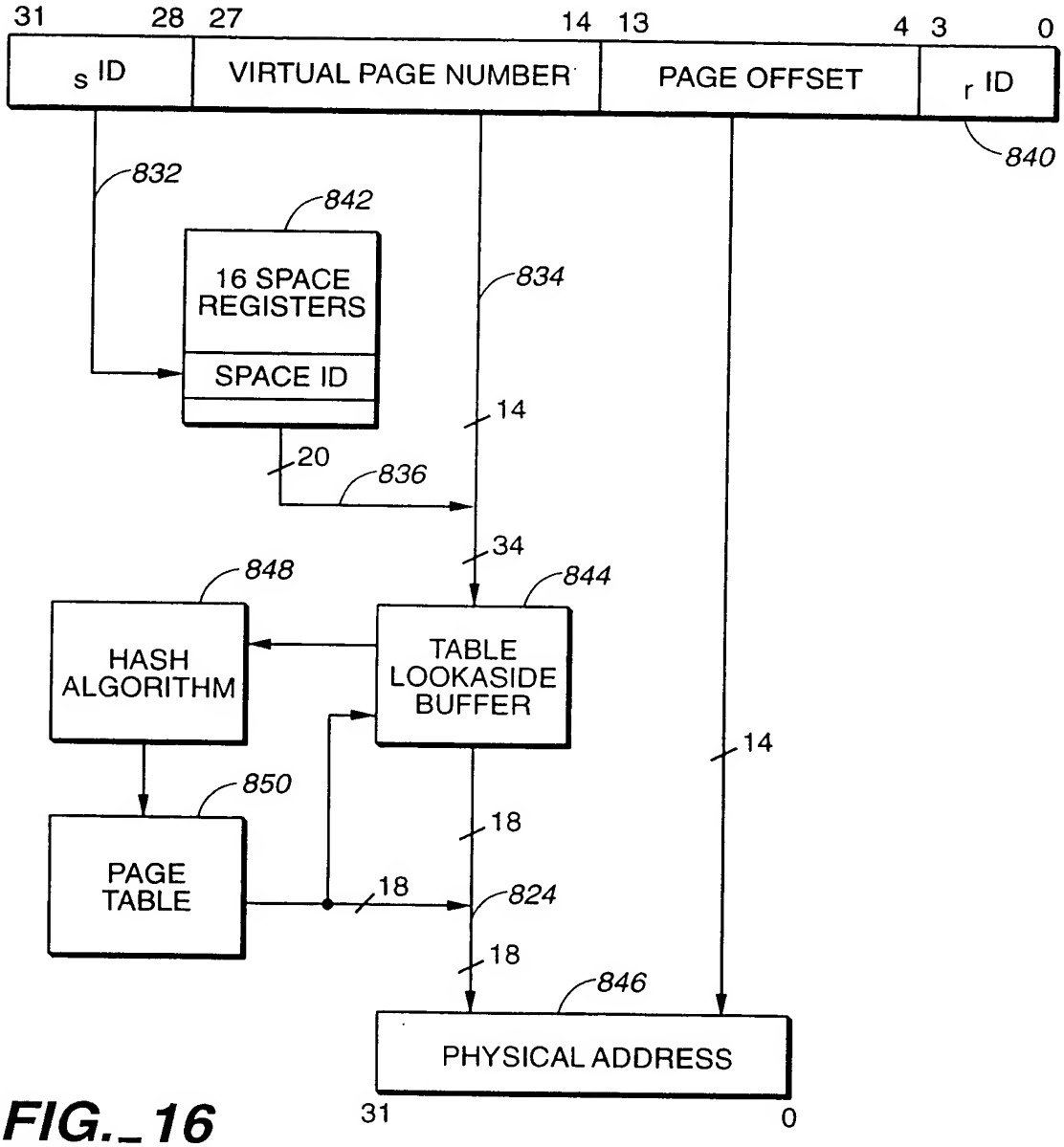

FIG._16